

**ENGR 270 Digital Design, Cuyamaca College**  
Spring Semester 2012, Section 9193  
Monday, Wednesday, 6 – 8:55, Rm F301

ENGR 270 Digital Systems will give you basic knowledge for the design and construction of combinational and sequential logic systems. In addition to the fundamentals, you will learn VHDL (VHSIC (Very High Speed Integrated Circuit) Hardware Description Language) to model circuits. In the lab you will implement your designs using discrete components, integrated circuits, and an FPGA (Field Programmable Gate Array).

**Instructor**

Dr. Duncan McGehee  
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Office Hours: MW 1 – 2:30 pm, MW 5:30 – 6 pm, Th 5 – 6 pm, or by appointment

**Units and Prerequisites**

4 units. Prerequisite: MATH 175 or 176.

**Text:** Fundamentals of Logic Design, 6<sup>th</sup> edition, Roth & Kinney, 2010, Cengage Learning, ISBN 0-495-47169-0.

**Other Required Supplies:** Lab notebook. This must be either cloth or spiral bound. Loose-leaf notebooks will not be accepted. I recommend that your notebook be quad ruled (graph paper rather than simply lined), and 8.5" x 11".

**Grading**

A: 90 - 100  
B: 80 - 89.9999  
C: 70 - 79.9999  
D: 60 - 69.9999  
F: < 60

Homework	15%
Midterm Examination 1	20%
Midterm Examination 2	20%
Final Examination	20%
Labs	25%

Note on grades:

There will be no make-up exams. If you MUST miss an exam, you MUST let me know BEFORE the exam (or bring a note from the police officer investigating the accident). If you do this, your final will be worth 40% of your grade. If you don't, you will receive a zero on the exam. If you miss both midterm exams, the second midterm exam will receive a zero. If you miss the final exam, you will receive a zero for it.

**Policies**

- 1) Always read the material to be covered in class *before* the lecture.
- 2) Always bring textbook and calculator to class.
- 3) Cell phones must be off and tucked away before lecture begins. This includes text messages transmitted or received.
- 4) Cheating. If I think you are cheating on an exam:
  - a) You will get a zero for that exam
  - b) I will invite you to withdraw from the class
  - c) Cell phones anywhere in evidence during an exam will be considered *a priori* evidence of cheating. I'll take a picture of your cell phone with my cell phone, give you a zero, and kick you out of the room.

**Important Dates**

3 February: Final day to add classes, or to drop without a 'W'.  
20 April: Final day to drop classes.

This course adheres to policies outlined in the Cuyamaca College Catalog. For further information, please see the section of the catalog entitled *Academic Policies*.

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Tentative schedule

Lesson	Date	Topic	Reading (BEFORE class)	Lab
1	23 Jan	Introduction, number systems		No lab
2	25 Jan	Number systems, binary arithmetic	Ch 1	No lab
3	30 Jan	Boolean algebra	Ch 2	Lab 0
4	1 Feb	Boolean algebra		Lab 0
5	6 Feb	Intro. to Logic Circuit Design, more Boolean	Ch 3	Lab 1 preparation
6	8 Feb	Minterm and maxterm expansions	Ch 4	Lab 1 preparation
7	15 Feb	Minterm and maxterm expansions		Lab 1
8	17 Feb	Karnaugh maps	Ch 5	Lab 1 due
	20 Feb	<b>Presidents' Day Holiday</b>		
9	22 Feb	Karnaugh maps		Lab 2 preparation
10	27 Feb	Multi-level gate circuits	Ch 7	Lab 2
	29 Feb	<b>Midterm Examination 1</b>		Lab 2 due
11	5 Mar	Multilevel gate circuits		Lab 3 preparation
12	7 Mar	Combinational circuit design	Ch 8	Lab 3 preparation
13	12 Mar	Multiplexers, decoders, and PLAs	Ch 9	Lab 3
14	14 Mar	Multiplexers, decoders, and PLAs		Lab 3 due
15	19 Mar	Latches and flip-flops	Ch 11	Lab 4 preparation
16	21 Mar	Flip-flops, continued		Lab 4 preparation
17	26 Mar	Registers and counters	Ch 12	Lab
18	28 Mar	Registers and counters		Lab 4 due
	2-6 April	<b>Spring Break</b>		
19	9 Apr	Clocked sequential circuits	Ch 13	Lab 5 preparation
	11 Apr	<b>Midterm Examination 2</b>		Lab 5 preparation
20	16 Apr	Clocked sequential circuits		Lab 5
21	18 Apr	State graphs and tables	Ch 14	Lab 5 due
22	23 Apr	State graphs and tables		
23	25 Apr	Reduction of state tables	Ch 15	
24	30 Apr	Reduction of state tables		Lab 6 preparation
25	2 May	Sequential circuit design	Ch 16	Lab 6 preparation
26	7 May	State machine design	Ch 19	Lab 6
27	9 May	State machine design		Lab 6 due
	14 May	<b>Final Examination</b>		
	16 May			Final project due

*subject to minor changes -*

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## Course Objectives (Expected Student Learning Outcomes)

Students will be able to:

- 1) Do arithmetic in the binary, octal, decimal and hexadecimal number systems and convert from one to another.
- 2) Design and build multi-level gate circuits, adders, multiplexers, decoders, and other combinational circuits starting from a verbal description, a truth table, or a Boolean output function. Apply Boolean algebra, Karnaugh maps, and “don’t care” conditions to simplify and optimize circuits.
- 3) Analyze a combinational circuit to determine the associated truth table and Boolean output function.
- 4) Explain the operation of a ROM (Read-only memory), PLD (programmable logic device), CPLD (complex programmable logic device), and FPGA (field programmable gate array).
- 5) Design and build flip-flops, registers, counters, and clocked sequential circuits (Moore and Mealy machines) starting from a verbal description, a state table, a state diagram, or a timing diagram.
- 6) Simplify sequential circuits through redundant state analysis, the judicious use of state assignments, and one-hot encoding.
- 7) Conduct state and timing analysis of sequential logic circuits.
- 8) Apply VHDL (Very High Speed Integral Circuit Hardware Description Language) to simulate and build combinational and sequential logic circuits.
- 9) Document all aspects of the design and testing of a digital circuit.

## ENGR 220 Exam Problem Grading Rubric (subject to modification)

Level		Description
5	100%	Answer is correct, main concepts and principles are clearly demonstrated. Solution is clear and logical. Truth tables, state tables, state diagrams, circuit diagrams, and optimized Boolean expressions are correct. Solution has been checked as thoroughly as possible.
4	88%	Same as level 5, but answer is incorrect due to a checkable math error. Answer is nevertheless credible (not obviously wrong).
3	80%	Same as level 4, but some part of the answer is obviously wrong.
2	72%	Answer is incorrect due to a minor conceptual error, or due to several algebraic errors or errors in execution. Main concepts and principles are clearly demonstrated, and the solution is clear and logical. Answer may or may not be credible.
1	40%	Answer is incorrect. Some evidence of understanding of main concepts and principles, but solution is not clearly demonstrated. This includes missing diagrams or tables. This is the highest grade possible the reasoning is absent <i>even if the answer is correct</i> .
0	0%	Scant evidence of understanding of the main concepts and principles.

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**Homework**

Each homework set will be worth 10 points. The grade will be based both on **completeness** and **presentation** as follows:

**Completeness – 5 points**

Level	Points	Description
4	5	Homework is complete, all problems have been done, or at least seriously attempted. Work is neat and legible. Each problem is on its own page.
3	4	Same as level 4, but problems are not each on their own page.
2	3	Several problems have not been attempted (an attempt means more than just writing down the problem). Work is neat and legible.
1	1	Only a few problems have been attempted. Work is neat and legible.
0	0	Homework was not handed in, or makes little sense, or is illegible.

**Presentation – 5 points**

I will choose one problem in the homework set to examine more closely. It will be graded according to the following rubric:

Level	Points	Description
4	5	Problem is clearly stated, with a clear solution that is easy to follow. Truth tables, Boolean expressions, and circuits are provided as needed.
3	3	The problem is clearly stated, and there is a solution, but it is not easy to follow. Truth tables, Boolean expressions, and circuits are provided as needed.
2	2	A solution has been reasonably attempted, but not successfully completed. Truth tables, Boolean expressions, and circuits may be missing.
1	1	Only the problem statement is present. No solution has seriously been attempted. Or there is a solution, but it is identical, or suspiciously similar, to the one in the solution manual.
0	0	The problem has not been attempted, or makes very little sense.

**Additional comments regarding homework:**

1. I will devote no more than two minutes to grading your homework set. That's enough for me to assess completeness and presentational clarity. However, it is not enough for me to figure out where you went wrong on a problem unless your presentation is crystal clear. Therefore, if you have questions about the homework, please come see me during office hours. I will also be providing solutions (on-line or in the library) *after* the homework has been submitted.
2. I will drop your lowest homework grade.

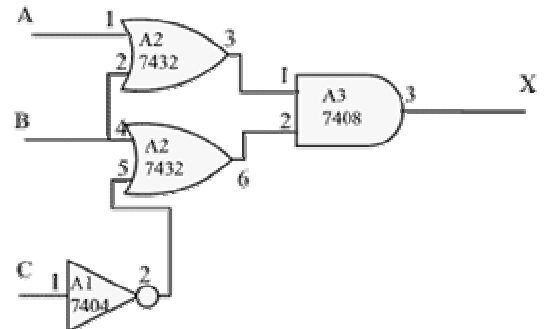
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**Labs**

- 1 Labs are generally 2 weeks long, with the first week devoted to planning – preparing truth tables, designing circuits, etc., and the second week devoted to actually assembling and testing the circuits.
- 2) The product of each lab is the lab report written in your lab notebook, which will be submitted for grading at the end of the lab period on Wednesday of the second week. The lab report should include the following parts. These will be written during the week of planning, and completed during the week of testing and experimentation:
  - a) Lab number (e.g. Lab 3)
  - b) Your name and your lab partner's name.
  - c) Overall objective of the lab. This should be brief and in your own words. Don't write something cute like "get a good grade". Instead, think about what the lab is meant to examine or explore. So perhaps something like: "Objective: Examine the function of multiplexers and other MSI components".
  - d) Theory and Procedure, on a problem-by-problem basis, including the following for each problem:
    1. Problem statement (you may copy the statement given in the assignment).
    2. Truth tables or state tables and diagrams for any analysis and design. Leave room on the tables for experimental data.
    3. Optimized Boolean function for the outputs.
    4. Schematic diagrams with pin numbers, or VHDL code when appropriate.
    5. Leave room for comments and results.
- 3) Further comments about your lab notebook:
  - a) Lab notebooks should always be written in pen, never pencil.
  - b) It is recommended that you only write on the right-hand pages of the lab notebook, leaving the left hand side for later corrections if needed.
  - c) Number and date each page as you use it. If you follow the advice of only writing on the right side, you can label the left side pages with a page number followed by the letter b. So for example if your notebook is open to page 10 on the right, 9b would be on the left.
  - d) All errors should be crossed out, in such a way as to leave legible the work under the cross-out. NEVER ERASE, and NEVER SCRIBBLE OUT the work so that it can't be read. Corrections can be placed on facing pages, or on following pages. In all cases, when you cross something out, indicate where the correction can be found. If errors on drawings are minor, the correction may be made directly on the drawing.
- 4) The second week of the lab will be very fast paced. You must work swiftly and efficiently.
  - a) All working circuits must be demonstrated to the instructor, and his initials obtained on or near the truth table.
  - b) If the instructor is not available, you may obtain the signature of another student who has successfully built that circuit. In such a case, the student must first print his/her name, then initial it.

Be concise in your lab report, but do not omit important details. Use the following criterion for how much to include: *Using only your notebook, a person with no more experience than you should be able to repeat the lab and verify the conclusions.*

**Note:** Schematic diagrams with pin numbers are required for every design.



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In general, labs will be worth 20 points each, with the exception of Lab 0, which will be worth 10 points. The points will be determined according to the following rubric.

## Tentative Lab Grading Rubric (this may evolve with time)

Level	Points	Description
5	20	Lab is complete, written in ink in a bound notebook. Good title, all group members listed, all pages dated. Each section of the lab is properly described, contains all relevant schematics, complete tabular data, schematics as needed. All circuits test out correctly. The work indicates a good understanding of the principles and major concepts of the lab.
4	17	Same as 5, but not in bound notebook. Or missing very minor things (such as all pages not being dated, or group members not listed). Lab is otherwise complete and well done.
3	14	Same as 4, but not all parts of lab were completed by the end of the lab. Lab is mostly completed, and those parts that are complete are done well, and indicate a good understanding of the principles and major concepts. Or, if the lab is complete, it contains at least one major conceptual error, or several minor ones, or a question or two left unanswered. Minor misunderstanding of how the lab works or what its purpose is.
2	12	Lab lacks major components, or contains several major conceptual errors, or reflects a major misunderstanding of equipment use, or several questions left unanswered. Otherwise the lab work appears to reflect a familiarity with the core concepts.
1	6	The lab both lacks major parts, and contains a variety of major conceptual errors. Or most questions were left unanswered. Or there is a significant inability to use the lab equipment. Some evidence of effort, but generally very disappointing.
0	0	Lab makes very little sense, or contains very little work.

I will be using checklists to grade the labs. What follows is a generic version of the checklist I'll develop for each lab. You can use the checklist to make sure you've covered everything.

### Generic Checklist for grading ELEC 201 labs

#### Overall

- \_\_\_\_\_ Title
- \_\_\_\_\_ Names of all individuals in lab group.
- \_\_\_\_\_ Overall lab objective
- \_\_\_\_\_ All pages numbered and dated.

#### For each section of the lab:

- \_\_\_\_\_ Problem statement
- \_\_\_\_\_ Circuit diagrams and schematics
- \_\_\_\_\_ Truth table or state tables
- \_\_\_\_\_ Room for experimental results
- \_\_\_\_\_ Optimized Boolean expressions for each output, as appropriate
- \_\_\_\_\_ Circuit diagrams with labeled pins
- \_\_\_\_\_ Additional Comments relating to the experiment – what you noticed, things that bothered you, etc.
- \_\_\_\_\_ Instructor's signature indicating successful demonstration